USING SUBMODELING TECHNIQUE TO UNDERSTAND PASSIVATION CRACKS IN MICROELECTRONIC DEVICES Pre-processing with ANSA

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ABSTRACT - Electronic devices like integrated circuits (IC) are used for automotive applications. The plastic (in the most cases mold compound) encapsulated devices exposed to temperature cycling (TC) undergo an excessive mechanical stress due to different coefficients of thermal expansion (CTE) of the various materials used in the system.

The large difference in the CTE between mold compound (MC) on the one hand and silicon and lead frame on the other hand causes in the metallization layers thermally induced strains and consequently stresses.

An analysis of the strains (or stresses), as they occur after molding, under subsequent tests, e.g. temperature cycling, and under realistic service conditions revealed that plastic encapsulated ICs show two main failure mechanisms, which are thermo-mechanically induced: metal shifts and passivation cracks.

This paper presents the computation of the thermally induced strains and stresses by using the Finite Element Method (FEM). The very small feature size of the passivation layer comparing with the global package size is one of the greatest problems in the application of the mentioned method and was solved by using submodeling.

Submodeling is a finite element technique that can be used to obtain more accurate results in a particular region of a model. A finite element mesh may be too coarse to produce satisfactory results in a given region of interest. The results away from this region, however, may be satisfactory. By using submodeling to generate an independent, more finely meshed model of the region of interest only made in this case the computation of the strains and stresses possible.

The large possibilities provided by the software ANSA (Automatic Net-generation for Structural Analysis) allowed a time saving generation of the 3D geometry and mesh of the submodel.

Results obtained with the FEM show a very good agreement with the location of passivation cracks as detected by Scanning Electron Microscope (SEM). It was possible to understand the mechanism of crack occurrence and to deduce corrective actions in order to develop a robust design.

TECHNICAL PAPER -

INTRODUCTION

The object of our investigation is a chip produced for automotive electronics. It is a micro electronic component having a length of 16 mm, a width of 11 mm and a thickness of 3.25 mm (Figure 11).
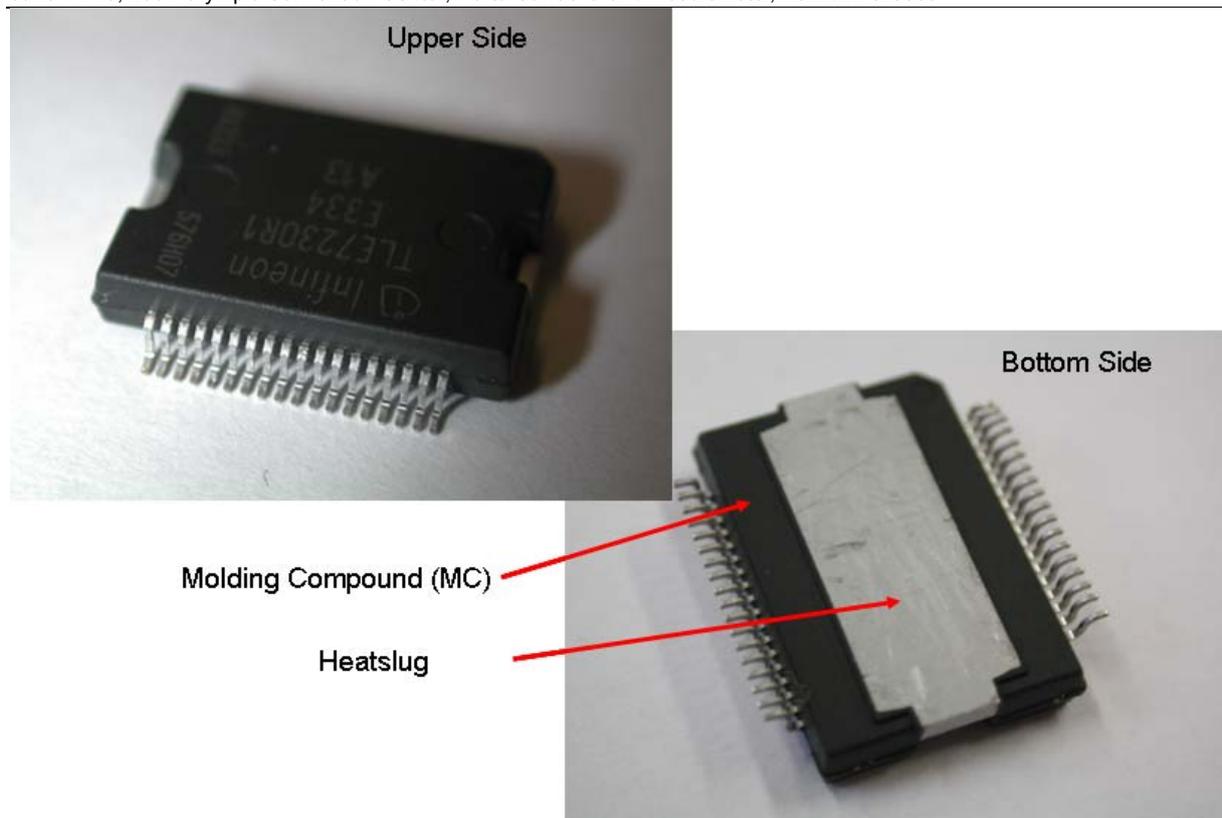
Figure 11: Examined object

This micro electronic component consists of a copper heat slug, the silicon chip, the lead frame and the molding compound. The latest serves for the protection against environmental influences like dust, humidity and chemical pollutants (Figure 12).
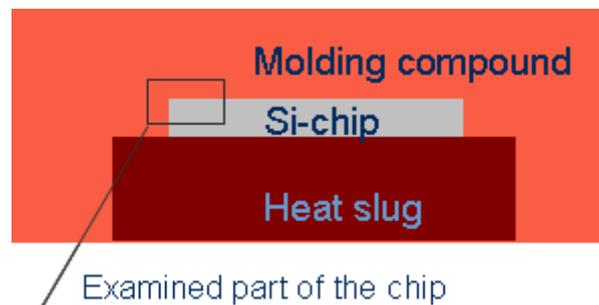

Figure 12: Longitudinal section of the examined object

To allow the contact of the individual electrical elements (i.e. transistors) with the exterior, several metal layers are needed. Isolators made of glass or ceramic are placed between the metal layers. Because the molding compound doesn't offer a 100 per cent protection, the metallization is protected with an additional passivation layer. In the presented example it consists of silicon nitride (Figure 13).
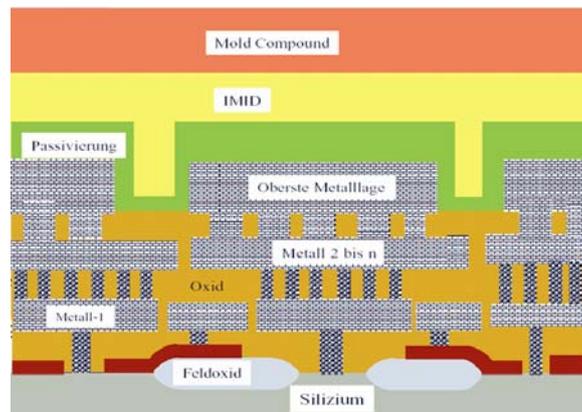
Figure 13: Metallization layers protected with an additional passivation layer

All these layers are applied one by one by chemical vapor deposition and/or sputtering at relatively high temperatures. After the production the wafer is sawed up and the individual chips are transferred to the final assembly.

The final assembly consists also of several steps. In this example the chip became soldered on the heat slug at temperatures over 300°C. After the cooling on ambient temperature the two parts become warmed and then embedded with molding compound at 175°C. After that the molded lead frames are cooled down to ambient temperature, the leads are plated and the trim and form process follows. Finally the devices are stored and delivered to the customer.

Consequently a device consists of different materials. The adhesion of the individual layers is particularly good. Very high shear stresses are induced in the component since the coefficients of thermal expansion of the layers are different. This leads in few cases to passivation cracks (Figure 14) even during the fabrication process.
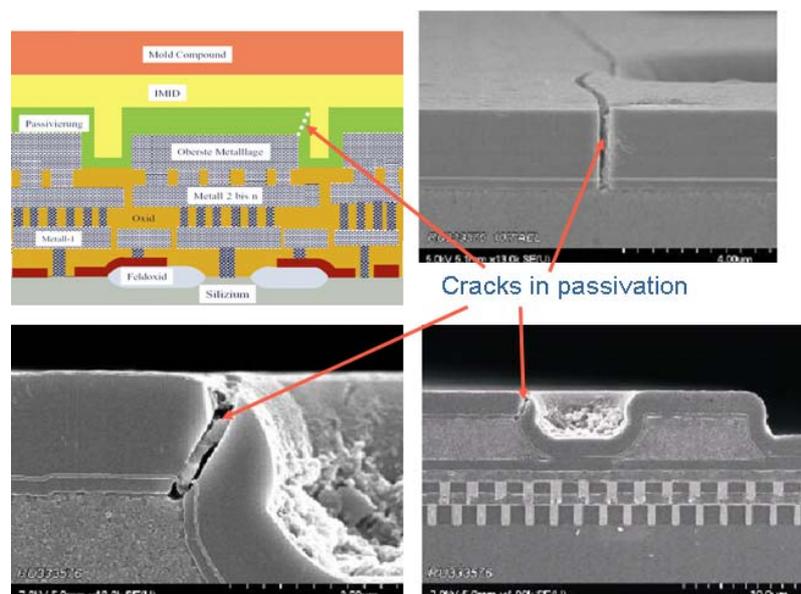

Figure 14: Scanning electron microscopy images of passivation cracks

BOUNDARY CONDITIONS

The majority of cracks occur during reliability tests like temperature cycling tests from -55°C to +150°C. This extreme temperature difference causes higher shear stresses and consequently leads to the failure of the passivation layer. Corrosion caused by humidity and chemical pollutants can act now and destroy the device. This leads to the failure of the presented micro electronic component.

The aim of the technology development is to develop robust products which are able to "survive" for e.g. 1000 temperature cycles from -55°C to +150°C.
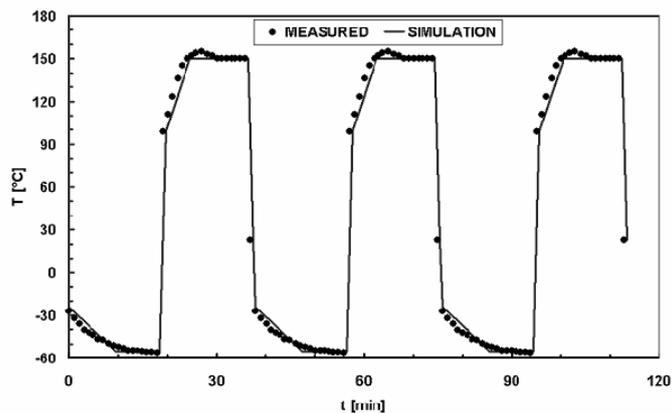

Figure 15: Three temperature cycles are shown exemplarily in this diagram.

The temperature profile during the temperature cycling test was measured in the immediate proximity of the electronic component and is represented in the (Figure 15) by the bulk symbols. A simplified temperature profile was simulated and represented in the diagram by the continuous line. The number of 1000 temperature cycles should correspond approximately to the average service time of a normally used car.

At the beginning of the project the components showed passivation cracks already after 100 temperature cycles (TC) (Figure 16).
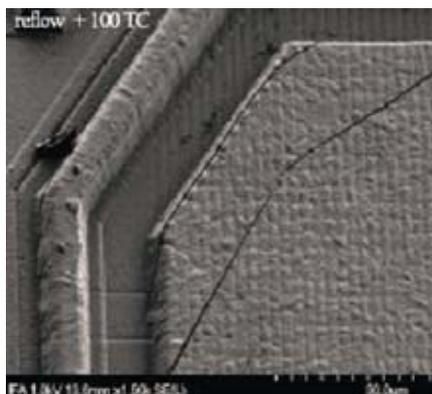

Figure 16: First visible cracks after 100 TC

MORE CRACK EXAMPLES

In Figure 17 and Figure 18 examples of passivation cracks are presented. Each figure shows the respective crack region in three different views. On the right hand side one can see a light microscopy (LM) image. It is hard to observe the cracks because the passivation layer as well as the oxide layers is transparent. In this picture one can recognize the individual metal layers. The cracks are well observable only in the scanning electron microscope (SEM) as shown in the bottom image.

Using these representations one can recognize only with difficulty the origin of the cracks. No suggestions for improvement can be derived from it. Such images can be made only at room temperature. The behavior at higher or lower temperatures can unfortunately not be derived from this representation. A FE simulation is the only possibility for a better understanding of the state of stress both at room temperature as well as at other temperatures.

On the left hand side top picture the FE model of the metal3 layer is shown. The area studied is approximately in the middle of the FE model.
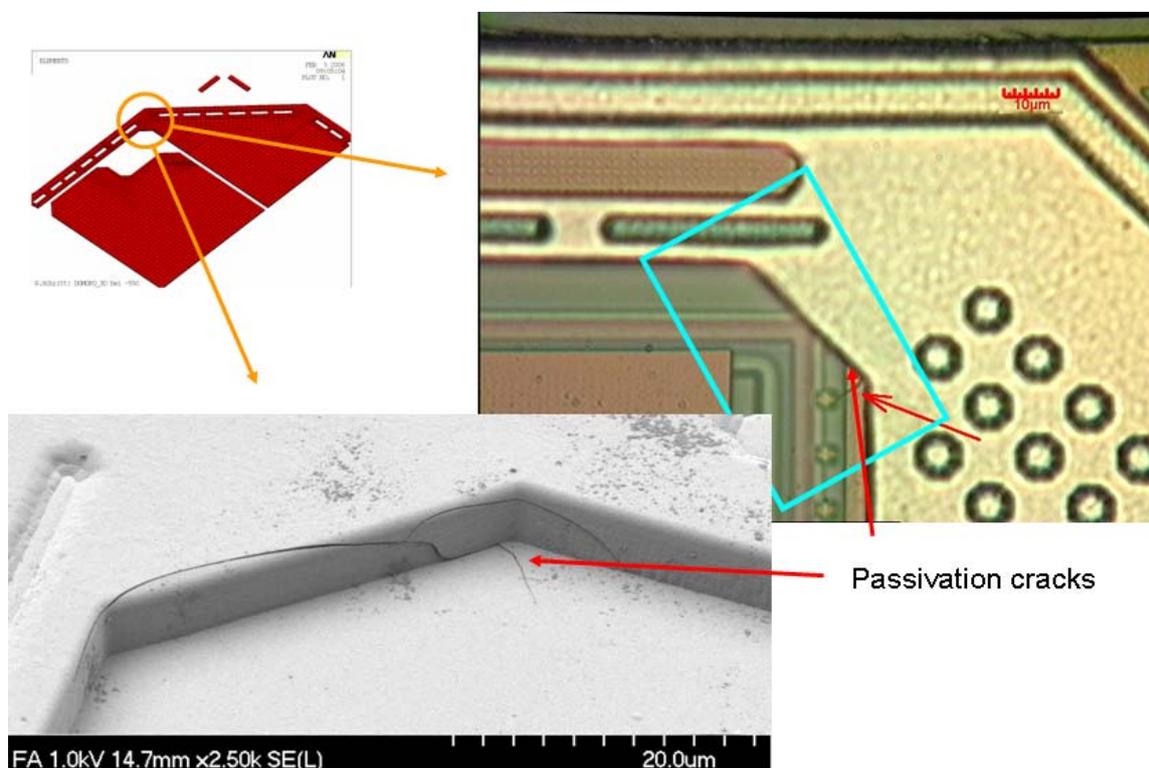

Passivation cracks

FA 1.0kV 14.7mm ×2.50k SE(L)   20.0um

Figure 17: LM and SEM image of a crack region and the corresponding FE-Mesh of the metal 3 layer

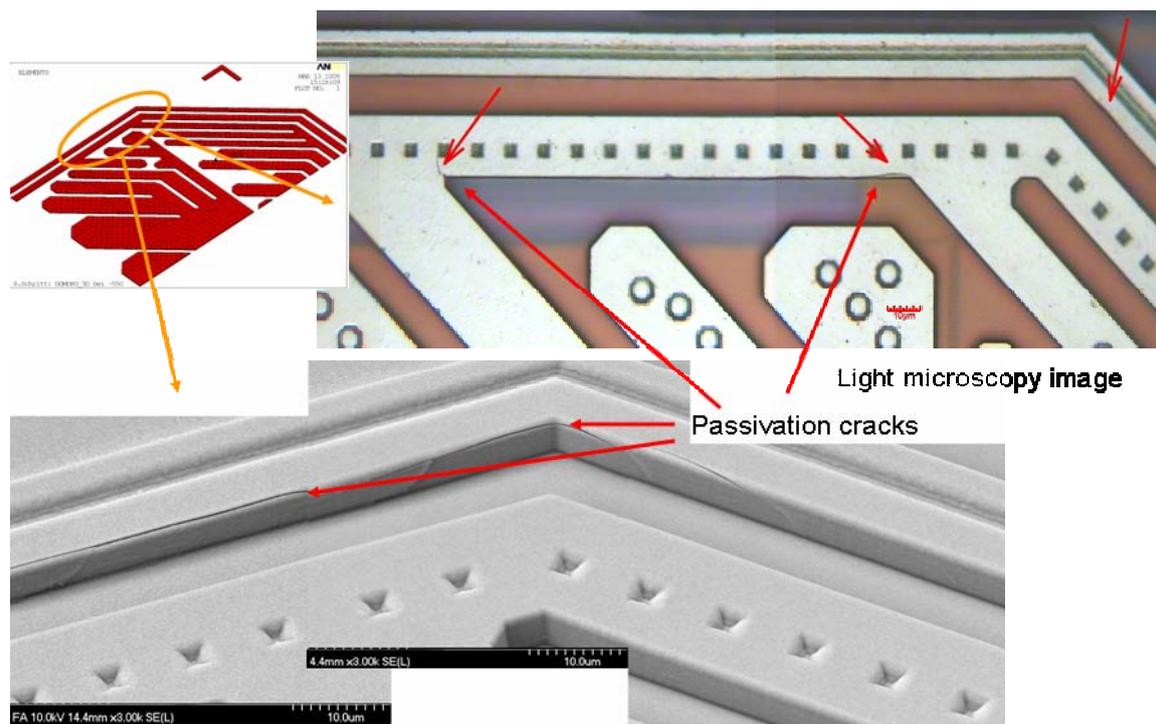The crack regions shown in Figure 17 and Figure 18 have been studied by FE analysis.

Figure 18: LM and SEM image of a crack region and the corresponding FE-Mesh of the meta 3 layer

In the FE simulation the production steps were considered because materials like solder and molding compound show a high temperature, time and stress dependency. Following production steps where simulated:

1. Wafer fabrication
2. Package fabrication
   - Silicon die (chip) attached at 305°C
   - Storage at room temperature for a few hours (simulating the time before wire bonding and embedding in mold compound)
   - Mold process at 175°C
   - Post mold cure process at 175°C
   - Storage at room temperature for a month (simulates storing at the manufacturer and transport time to the customer)
3. Simulation of one temperature cycle
   - Cooling down to -55°C and storage for 10 minutes
   - Heating up to +150°C and storage for 10 minutes
   - Cooling down to room temperature

Due to the limitation of the computer capacity only one temperature cycle could be simulated in the 3D model.

SUBMODELING

The stresses in the shown crack regions should be calculated as exactly as possible. For this purpose a fine meshing of the structure is required.
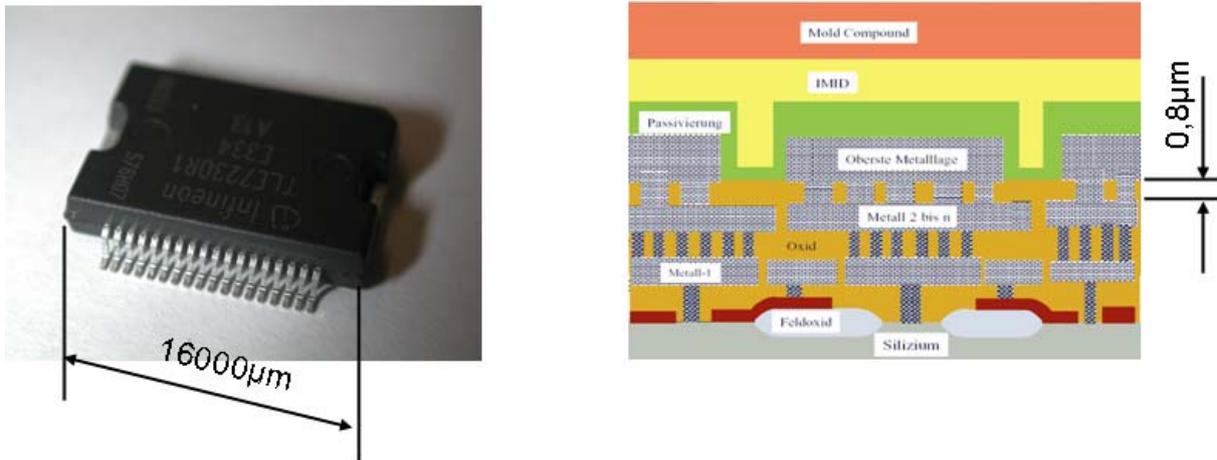

Figure 19: Ratio between longest and shortest line

Because of a ratio between the longest and shortest line of approx. 20000, many elements would be generated during the meshing of this micro electronic component (Figure 19). A simulation would be only possible on a mainframe computer. To avoid this obstacle, in the simulated examples a submodel technique in two steps was used.

Submodeling is a finite element technique (1) that can be used to obtain more accurate results in a particular region of a model (Figure 20).
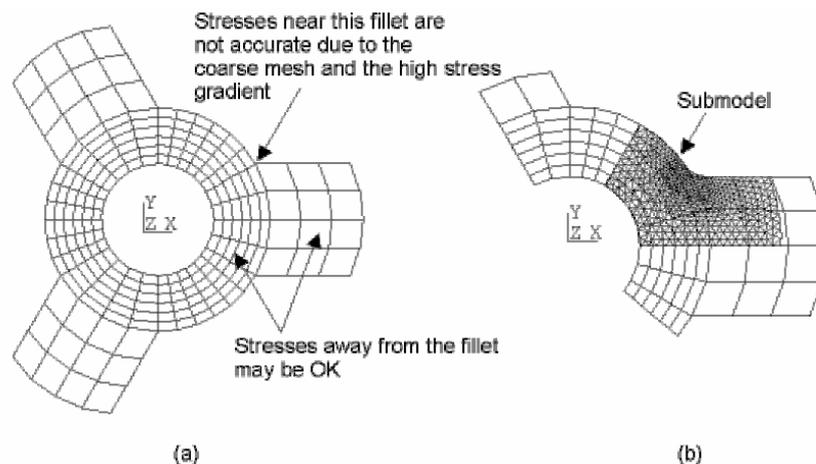

Figure 20: Submodeling technique

(a) Coarse meshed model
(b) Fine meshed submodel, superimposed to the coarse model

Submodeling is also known as the **cut−boundary displacement** method or the **specified boundary displacement** method. The cut boundary is the boundary of the submodel which represents a cut through the coarse model. Displacements calculated on the cut boundary of the coarse model are specified as boundary conditions for the submodel. Submodeling is based on **St. Venant's** principle, which states that if an actual distribution of forces is replaced by a statically equivalent system, the distribution of stress and strain is altered only near the regions of load application.

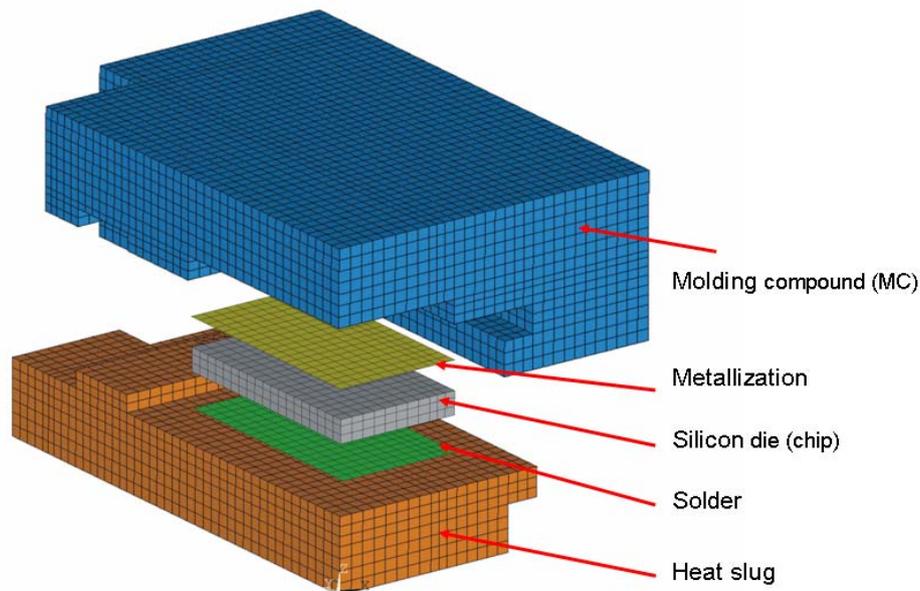As already mentioned, this micro electronic component consists of several parts (Figure 21).

Figure 21: 3D FE coarse model

The stresses in the metallization layers are of special interest, but the modelling of the individual layers is not possible in the coarse model. Subsequently a substitute layer was used instead of this layer structure. The material properties of this substitute layer were derived from the material properties of the layer structure.

Firstly the introduced approach was verified in a 2D example. The 2D model and its position in the 3D model are presented in (Figure 22). The big aspect ratios are pointed out again.
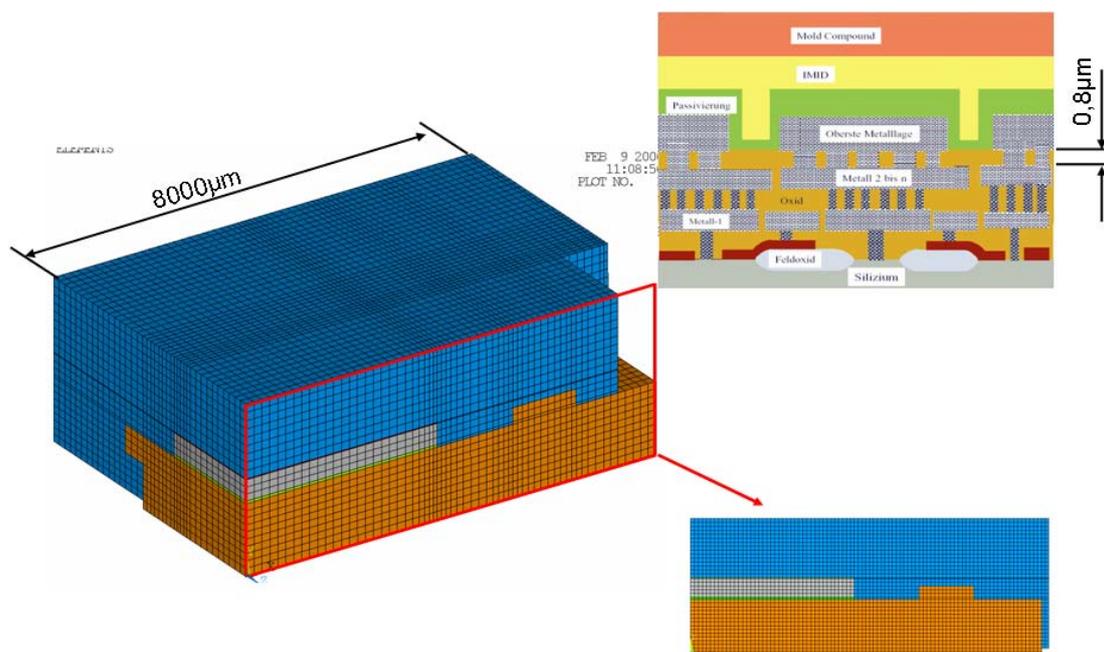
Figure 22: 3D and 2D coarse models

The coarse model, the 1st submodel and the 2nd submodel are shown in the figure below. The relative position of the individual models are pointed out by the rectangles. (Figure 23)
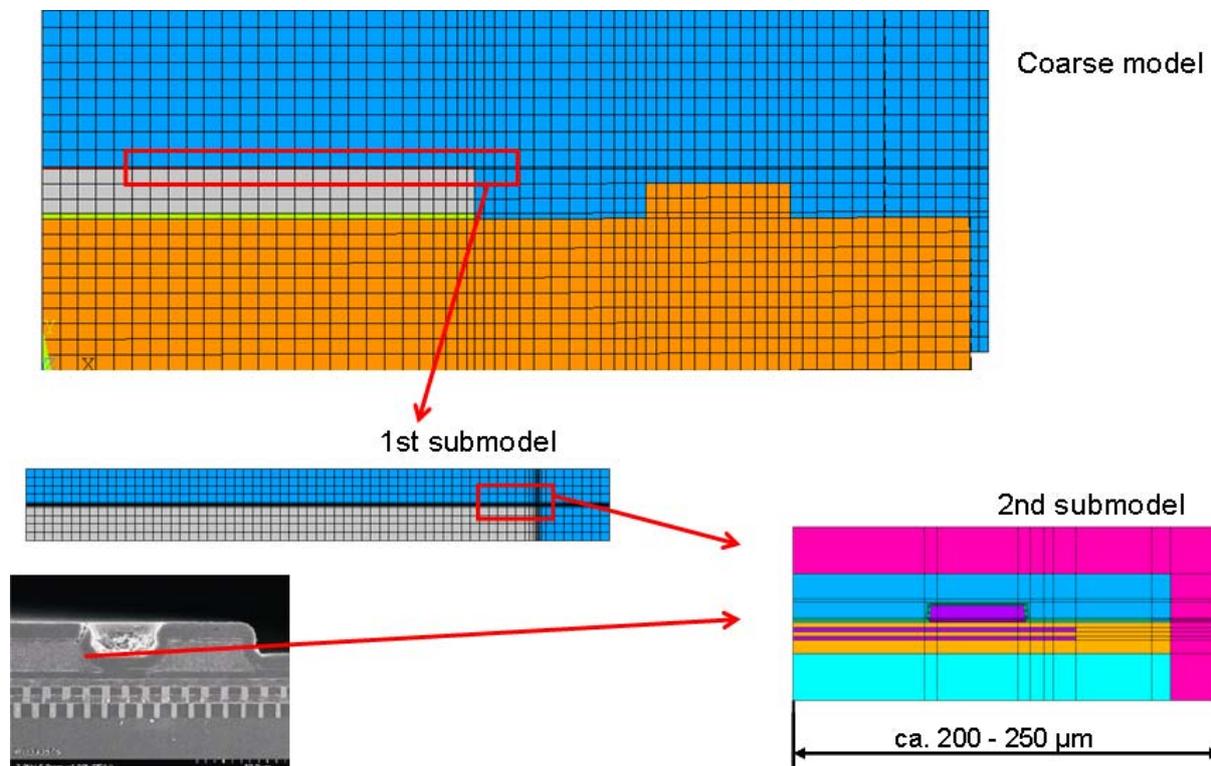

Figure 23: 2D-model of the chip – Coarse model, 1st and 2nd submodel

The 2nd submodel was created starting from the SEM picture presented in Figure 24. With this submodel first conclusions could be drawn regarding crack behavior of the studied cross section. In the submodel the aspect ratio of the longest too shortest edge was at most 250 μm to 0.8 μm. This would correspond to a ratio of at most 312,5. The obtained results allow planning and implementation of the 3D simulation.

The picture in Figure 24 represents a cross section through the 2nd submodel. It is important to include parts of silicon and molding compound in the model.
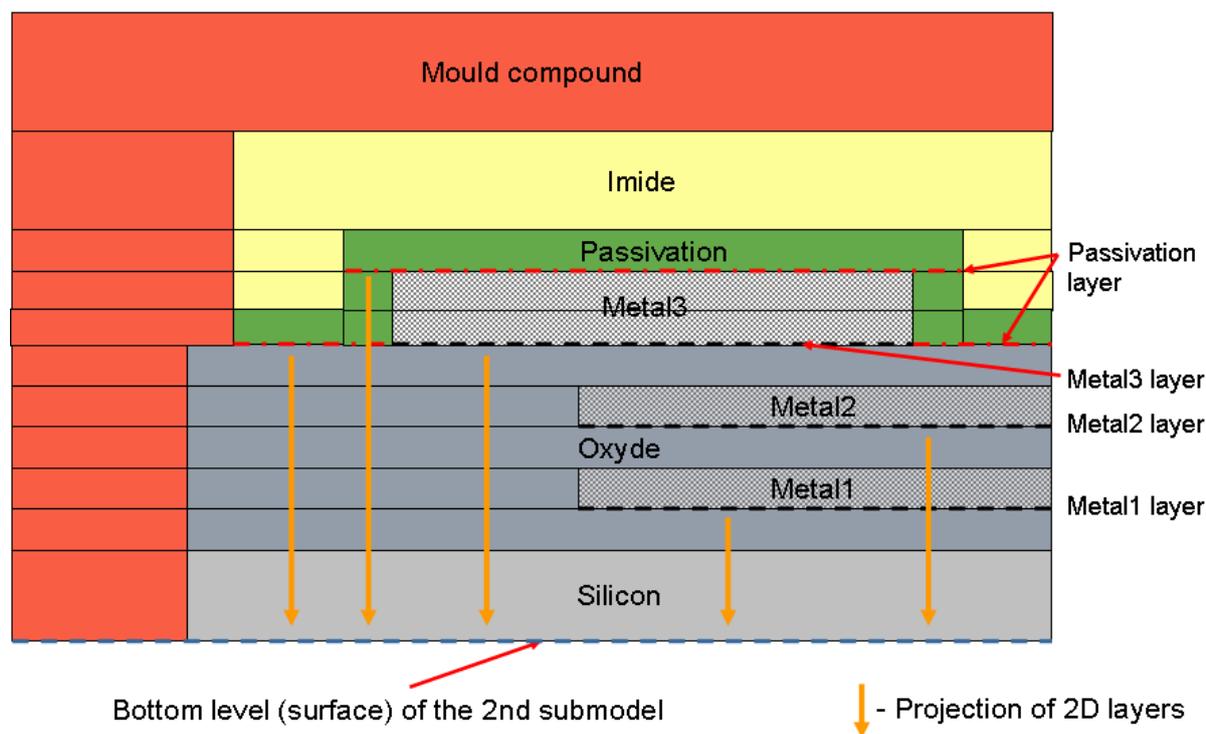

Figure 24: Cross section through the 2nd submodel

Using this cross section, the approach to the construction of the 2nd 3D submodel can be explained.

The information of the 2D representation of the three metal layers has been obtained from the E CAD tool of the layout developer. Unfortunately, only the structure of the conductors and its spatial position could be derived from this data. Consequently the 2nd 3D submodel could be created only by extrusion technique. Before the extrusion, the 2D information obtained from the layout tool had to be projected firstly onto the bottom level of the 2nd submodel. The projection of the 2D-Layers on the bottom surface is represented by the orange arrows.

In the presented example the six layers shown in (Figure 25) on the left hand side were projected onto the base of the 2nd submodel. The upper three layers are taken from the E-CAD tool of our customer. The lower three were generated in ANSA.
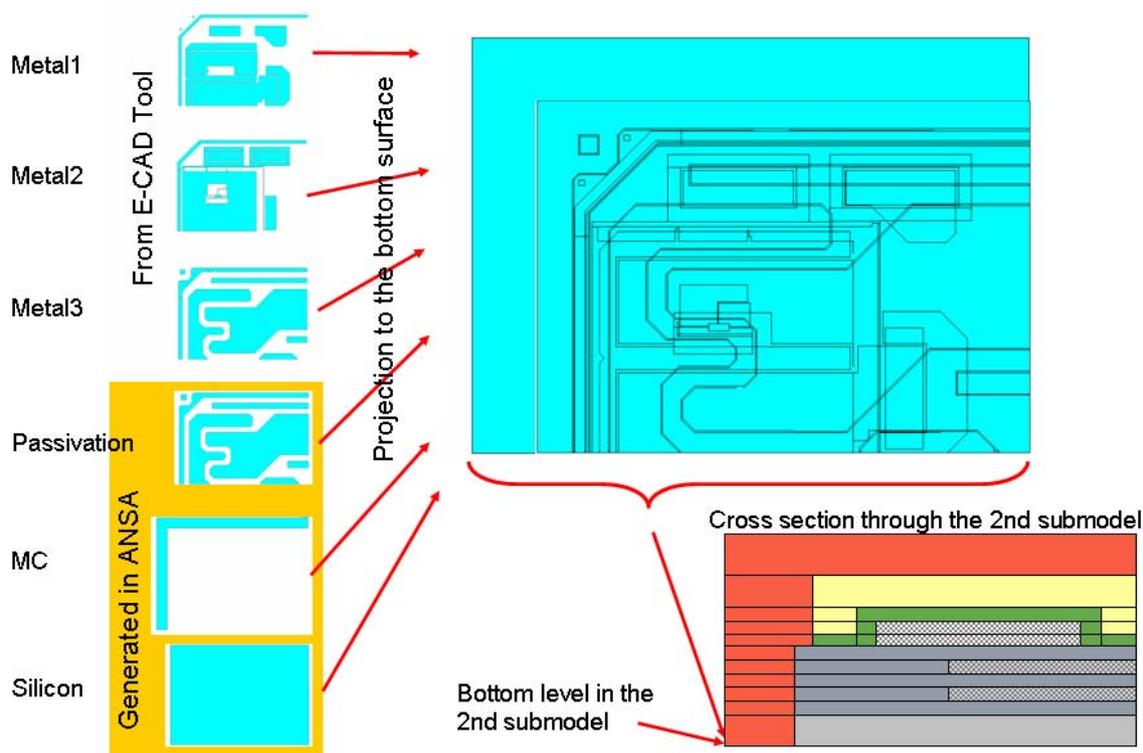
Figure 25: Projection to bottom surface

In the next step the meshing of the base was carried out (Figure 26). It is obvious that the obtained mesh is very sophisticated and it is very hard to assign the elements to the individual layers.
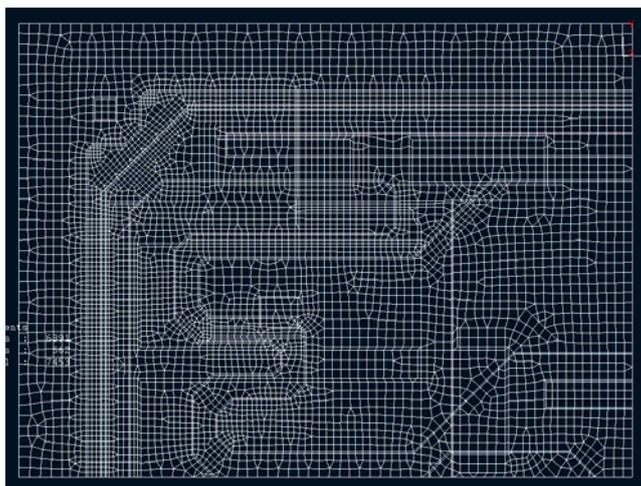

Figure 26: Meshed bottom surface

The topography of the three metal layers and the passivation layer is in the most cases very complex. The selection of the elements for the three metal layers was difficult and time consuming. The problem could be solved with ANSA very simply and very fast with the command TOPO > RM.DBL. The possibility of simply selecting the elements was one of the

reasons for the choice of this software. Parallel to the extrusion of the elements, the corresponding material properties were also assigned.
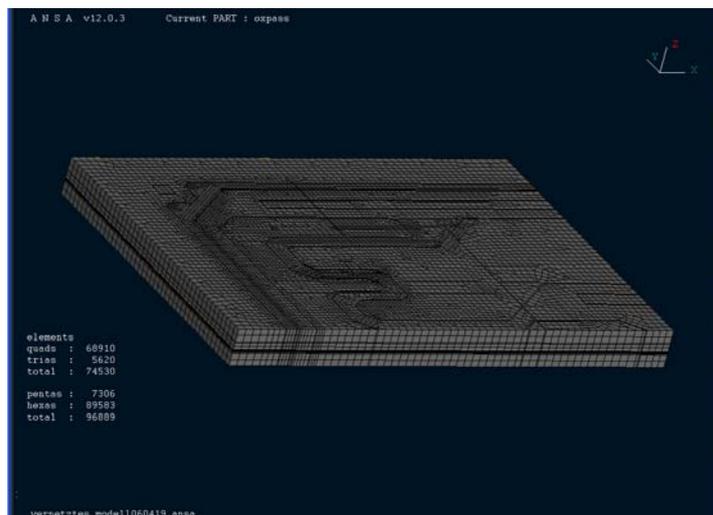

Figure 27: 3D FE-model generated by "step by step" extrusion

The simulated submodel had the size of about 750 µm to 500 µm (Figure 27 and Figure 28). The height was approximately 80 µm. The element size was reduced correspondingly in the areas where higher stress gradients were expected. Elements with midside nodes were chosen.
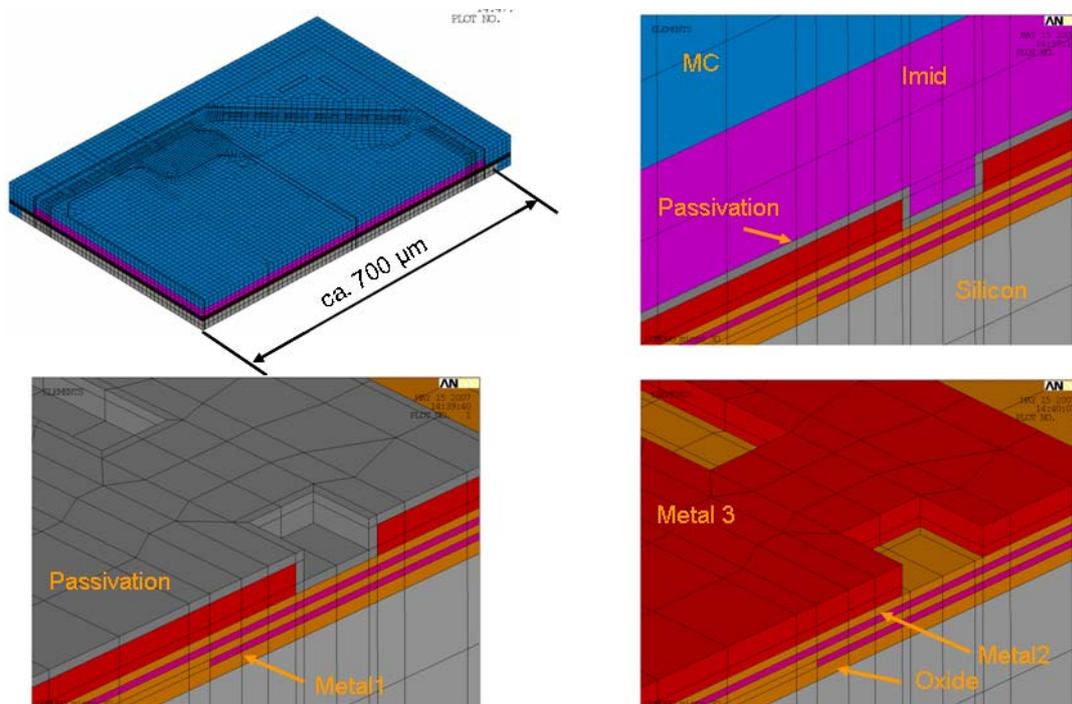

Figure 28: 3D FE-model of the crack region

3D SIMULATION OF THE CRACK REGION

In the next three figures the results of the thermo-mechanic evaluations carried out by ANSYS are presented. Since the studied passivation layer is a very brittle material, the 1st principal stress was evaluated here at -55°C (Figure 29, Figure 30 and Figure 31).
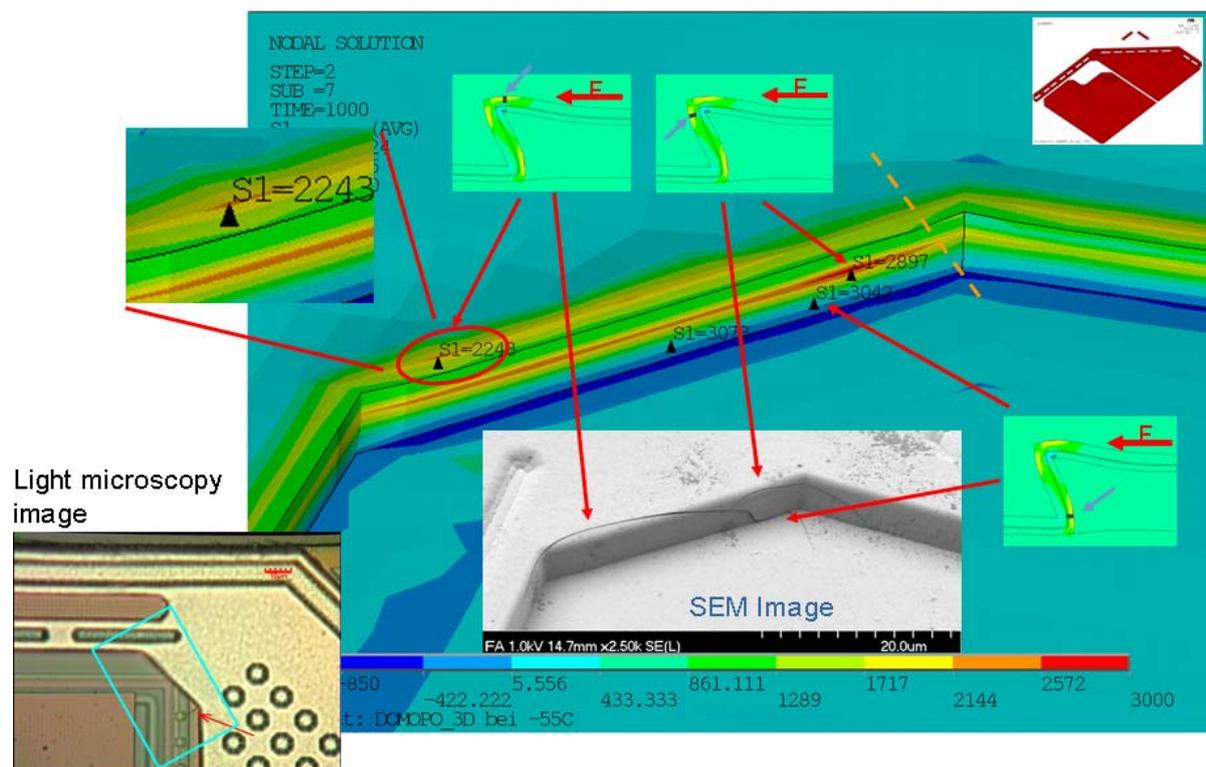

Figure 29: FE Results from 2D and 3D simulations compared with SEM Images

As mentioned above, simulations were conducted firstly in the 2D model. The result of these simulations is represented in the small windows. The simulated 2D cross section lies parallel to the direction of the forces. This corresponds approximately to the direction in the 3D submodel marked with the orange dashed line (Figure 29).

Using the 2D simulations a view into the states of strain and stress of this characteristic cross section could be obtained. With these recognitions the results in the 3D model could be better understood. In the 2D model three areas with very high principal stresses can be identified. We could recognize the stress peaks also in the 3D submodel in similar regions. In addition, the positions of these stress peaks show a very good agreement with the observed crack locations.

A good agreement of the results of simulation could also been observed with the SEM images in the submodel presented on (Figure 30). The stress peaks were compared with the actual crack locations in the region near the edge of the aluminum lines. The agreement is very good.
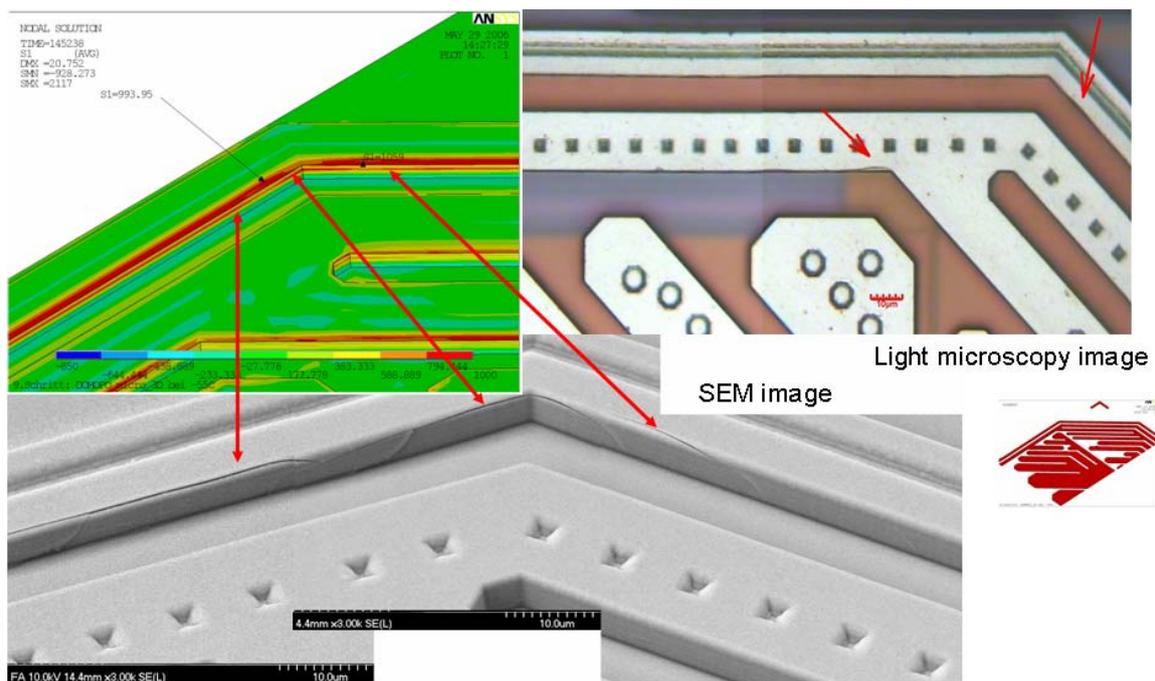
Figure 30: FE Results from 3D simulations compared with SEM Images

In Figure 31 another interesting comparison is presented. The position of the three stress peaks at the conductor edge agrees very well with the position of the three cracks on the SEM image.
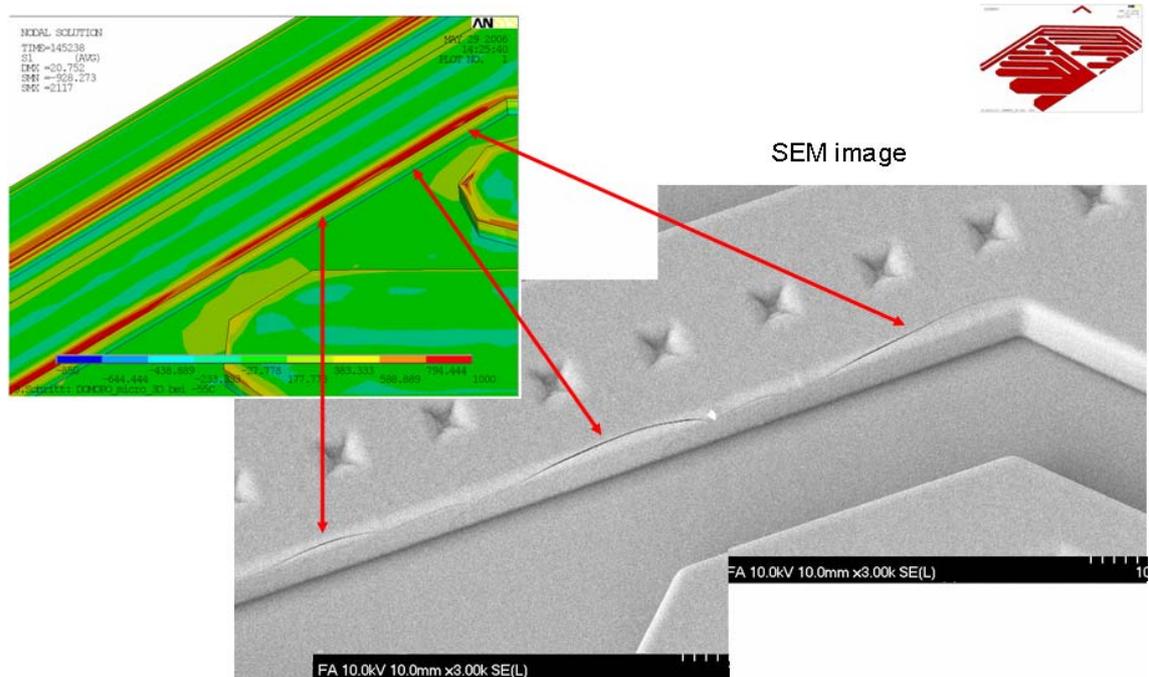

Figure 31: FE Results from 3D simulations compared with SEM Images

CONCLUSIONS

It could be shown that in spite of such extremely small structures, the 3D FE simulation can provide good results.

The location of maximum stresses shows a good correlation to the crack position observed experimentally. Thus the starting point of the passivation cracks can be predicted by FEM simulations. Additionally the influence of passivation topography on the maximum stress could be simulated and recommendations for new "Design Rules" could be deduced.

These results have a substantial contribution to the understanding of the thermo-mechanical behavior of 2 μm thick passivation layers.

The simulations introduced here were only the top of the iceberg. Basis for these good results was the very thorough examination of the material behavior of the individual layers.

Further simulations and investigations are required to be able to predict the failure of the investigated structures.

The benefits for the device supplier are obvious. The robustness and reliability of micro electronic devices for automotive application could be improved.

REFERENCES

(1)   Ansys, Inc., Canonsburg: "Advanced Guide", ANSYS Documentation, version 10